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Claims

[c1] 1. A semiconductor resistor device comprising a plurality of alternating conductive film and insulative film layers, at least two of the conductive film layers being electrically connected in parallel to provide for high current flow through the resistor device at RF frequencies with increased temperature and mechanical stability.

[c2] 2. The semiconductor resistor device as claimed in Claim 1, wherein said plurality of alternating conductive film and insulative film layers are in a planar orientation, said insulative film layers serving to limit current flow in a direction perpendicular to an insulator film surface.

[c3] 3. The semiconductor resistor device as claimed in Claim 1, wherein said plurality of conductive film and insulative film layers are in a trough orientation.

[c4] 4. The semiconductor resistor device as claimed in Claim 1, wherein each said conducting film layer comprises a metal material selected from the group consisting of Ta, TaN, Ti, TiN, W, and WN.

[c5] 5. The semiconductor resistor device as claimed in Claim 1, wherein a conducting film layer includes a resistive

material having a temperature coefficient of resistance (TCR) value, wherein at least two of the plurality of conductive film layers include materials having different TCR values to provide a desired effective temperature coefficient of resistance.

[c6] 6. The semiconductor resistor device as claimed in Claim 5, wherein a desired effective temperature coefficient of resistance is substantially 0 ppm/EC.

[c7] 7. A high current resistor device comprising a plurality of alternating refractory metal films of high sheet resistance and insulator film layers, wherein insulator films provide vertical self-ballasting, and said metal film layers exhibit a lateral self-ballasting effect created by the high resistance of the refractory metal.

[c8] 8. The high current resistor device as claimed in Claim 7, wherein the refractory metal film layers reduces skin effect at high frequencies and results in a self-ballasting effect.

[c9] 9. The high current resistor device as claimed in Claim 7, wherein said internal lateral and vertical self-ballasting provides more uniform current flow and reduces thermal stress, thus, increased current density and high peak temperatures are obtainable.

[c10] 10. The high current resistor device as claimed in Claim 7, wherein said metal film layers includes materials having different TCR values to provide a desired effective temperature coefficient of resistance.

[c11] 11. The high current resistor device as claimed in Claim 7, wherein said plurality of alternating refractory metal film layers of high sheet resistance and insulator film layers are configured as one of a planar multi-stack structure or trough structure.

[c12] 12. The high current resistor device as claimed in Claim 11, further comprising independently connecting different metal film layers to customize a resistance value.

[c13] 13. A method of forming a semiconductor resistor structure comprising the steps of:

a) providing an interlevel dielectric material structure;

b) etching a trough structure in said dielectric structure;

c) depositing a layer of conductive material having lateral and vertical portions in said trough structure;

d) depositing a layer of insulator material having lateral and vertical portions above said layer of conductive material in said trough structure;

e) alternating deposition of conductive and insulator

material layers according to steps c) and d) to form said resistor structure having desired properties tailored according to types and thicknesses of said conductive and insulator materials; and,

f) forming a via structure to connect one or more vertical portions of said conductive film layers of said resistor structure to an adjacent wire level.

[c14] 14. The method according to Claim 13, wherein the alternating conductive layers comprise a refractory metal having a high sheet resistance.

[c15] 15. The method according to Claim 14, wherein the alternating insulator film layers provide vertical self-ballasting, and the metal film layers exhibit a lateral self-ballasting effect created by the high resistance of the refractory metal.

[c16] 16. The method according to Claim 13, wherein the step of alternating deposition of conductive and insulator material layers according to steps c) and d) form a resistor structure having a desired net Temperature Coefficient of Resistance value.

[c17] 17. The method according to Claim 13, wherein the step of alternating deposition of conductive and insulator material layers according to steps c) and d) form a resis-

tor structure having a desired ESD value.

[c18] 18. A method of forming a semiconductor resistor structure comprising the steps of:

a) providing an interlevel dielectric material structure;

b) depositing a layer of conductive material in a planar orientation;

c) depositing a layer of insulator material having in a planar orientation above said layer of conductive material;

d) alternating deposition of conductive and insulator material layers according to steps c) and d) to form a multi-stack resistor structure having desired properties tailored according to types and thicknesses of said conductive and insulator materials; and,

e) forming one or more via structures to connect one or more of said conductive film layers of said resistor structure to an adjacent wire level.

[c19] 19. The method according to Claim 18, wherein the alternating conductive layers comprise a refractory metal having a high sheet resistance.

[c20] 20. The method according to Claim 19, wherein the alternating insulator film layers provide vertical self-ballasting, and the metal film layers exhibit a lateral self-ballasting effect created by the high resistance of

the refractory metal.

[c21] 21. The method according to Claim 18, wherein the step of alternating deposition of conductive and insulator material layers according to steps c) and d) form a resistor structure having a desired net Temperature Coefficient of Resistance value.

[c22] 22. The method according to Claim 18, wherein the step of alternating deposition of conductive and insulator material layers according to steps c) and d) form a resistor structure having a desired ESD value.

[c23] 23. The method according to Claim 18, wherein said step e) of forming one or more via structures to connect or more of said conductive films include utilizing single or dual damascene processes for forming said vias to connect one or more conductive films in parallel.

[c24] 24. A computer-aided design system comprising:

means for generating a parameterized cell (P-cell) data structure representing a semiconductor film element of a material type and thickness having desired properties in association therewith; and,

means for combining one or more P-cells to automatically generate a higher order p-cell data structure representing a semiconductor device tailored to

having desired one or more properties tailored according to inherited properties of the p-cells utilized in said combination.

[c25] 25. The computer-aided design system as claimed in Claim 24, wherein a tailored semiconductor device includes a resistor element having a desired resistance value.

[c26] 26. The computer-aided design system as claimed in Claim 24, wherein a tailored semiconductor device includes a resistor element having one or more desired properties selected from: a Temperature Coefficient of Resistance value; an ESD value; a degree of lateral and vertical resistor self-ballasting.

[c27] 27. The computer-aided design system as claimed in Claim 24, wherein said means for generating a parameterized cell (P-cell) data structure includes a graphical layout generator including an interface means enabling a graphical layout cell view of said resistor element, said interface means enabling user specification of parameters to be used in the generation of a P-cell data structure or higher order p-cell data structure representing said resistor element.

[c28] 28. The computer-aided design system as claimed in

Claim 24, wherein said means for generating a parameterized cell (P-cell) data structure includes a schematic layout generator including an interface means enabling a schematic cell view of said resistor element, said interface means enabling user specification of parameters to be used in the generation of a P-cell data structure or higher order p-cell data structure representing said resistor element.

[c29] 29. The computer-aided design system as claimed in Claim 27, further including means enabling the autogeneration of a circuit, said means utilizing p-cell or higher order p-cell data structures to be included in said circuit for enabling the tailoring of circuit performance according to user specification.

[c30] 30. A method of computer-aided design comprising the steps of:

a) generating a parameterized cell (P-cell) data structure representing a semiconductor film element of a material type and thickness having desired properties in association therewith; and,

b) automatically generating a higher order p-cell data structure by combining one or more p-cells, said higher order p-cell data structure representing a semiconductor device including one or more semiconductor film elements, said semiconductor device having desired one or

more properties tailored according to properties inher-
ited from the p-cells utilized in said combination.